

**Preliminary** 

# 1.6 GHz 20 W Flange Ceramic Packaged GaAs Power FETs

#### **FEATURES**

- 20 W Typical Power at 1.6 GHz
- 13 dB Typical Linear Power Gain at 1.6 GHz
- High Linearity: IP3 = 52 dBm Typical
- High Power Added Efficiency: Nominal PAE of 40 %
- Suitable for High Reliability Application
- Wg = 50 mm
- 100 % DC and RF Tested
- Flange Ceramic Package



#### **DESCRIPTION**

The TC2997A is a packaged Pseudomorphic High Electron Mobility Transistor (PHEMT) power transistor with input prematched circuits. The flange ceramic package provides the best thermal conductivity for the GaAs FET. All devices are 100% DC and RF tested to assure consistent quality. Typical applications include high dynamic range power amplifiers for commercial applications.

## ELECTRICAL SPECIFICATIONS (VDS = 10.5, IDS = 5A @ 1.6GHz)

Symbol	CONDITIONS	MIN	TYP	MAX	UNIT
$P_{1dB}$	Output Power at 1dB Gain Compression Point	42	43		dBm
$G_{\mathrm{L}}$	Linear Power Gain	12	13		dB
IP3	Intercept Point of the 3 <sup>rd</sup> -order Intermodulation*P <sub>SCL</sub> = 32 dBm		52		dBm
PAE	Power Added Efficiency at 1dB Compression Power		40		%
$I_{DSS}$	Saturated Drain-Source Current at V <sub>DS</sub> = 2 V, V <sub>GS</sub> = 0 V		12.5		A
$g_{\rm m}$	Transconductance at $V_{DS} = 2 \text{ V}$ , $V_{GS} = 0 \text{ V}$		9000		mS
$V_{P}$	Pinch-off Voltage at $V_{DS} = 2 \text{ V}$ , $I_D = 60 \text{ mA}$		-1.7		Volts
$BV_{DGO}$	Drain-Gate Breakdown Voltage at I <sub>DGO</sub> =15 mA	20	22		Volts
R <sub>th</sub>	Thermal Resistance		0.9		°C/W

<sup>\*</sup> P<sub>SCL</sub>: Output Power of Single Carrier Level.

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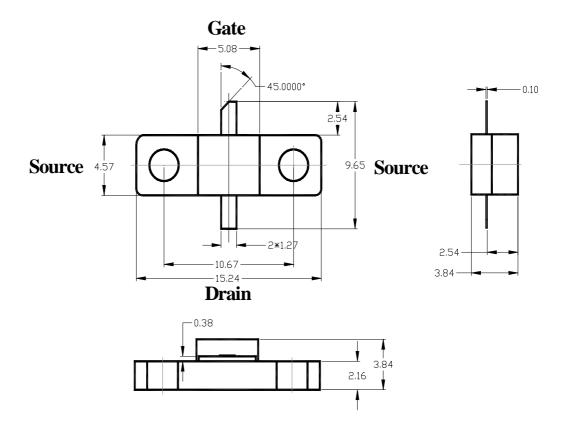
## ABSOLUTE MAXIMUM RATINGS at 25 °C

Symbol	Parameter	Rating
$V_{\mathrm{DS}}$	Drain-Source Voltage	12 V
$V_{GS}$	Gate-Source Voltage	-5 V
$I_{DS}$	Drain Current	$I_{ m DSS}$
$P_{in}$	RF Input Power, CW	37 dBm
$P_{\mathrm{T}}$	Continuous Dissipation	100 W
$T_{CH}$	Channel Temperature	175 °C
$T_{STG}$	Storage Temperature	- 65 °C to +175 °C

#### HANDLING PRECAUTIONS:

The user must operate in a clean, dry environment. Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. The static discharge must be less than 300V.

# FLANGE PACKAGE OUTLINE (in mm)



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